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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/270,256	03/15/1999	ILYA KLEBANOV	0100.9900440	2265

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EXAMINER	
YANG, RYAN R	

ART UNIT	PAPER NUMBER
2672	24

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/270,256	Applicant(s) KLEBANOV, ILYA	
	Examiner Ryan R Yang	Art Unit 2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6-11,13,17,18,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 6-11,13,17-18,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is responsive to communications: Amendment, filed on 5/13/2004. This action is final.

2. Claims 2, 6-11, 13, 17-18, 21 and 22 are pending in this application. Claims 21 and 22 are independent claims. In the Amendment, filed on 5/13/2004, claims 6, 7, 21 and 22 were amended, and claim 5 was canceled.

3. The present title of the invention is "Method and Apparatus for Rendering an Image in a Video Graphics Adapter" as filed originally.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 21, 2 and 6-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al. (5,657,046).

As per claim 21, Noble et al., hereinafter Noble, discloses a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 11 Video module #1 where a frame of video is as Figure 3 and a Video Module is considered a VGA);

rendering at least a first portion of the first frame of video at the first VGA in response to a first control signal, wherein the first control signal is a signal specifying a window location for displaying the active video (Figure 12 RAM Control to the Display

Memory Section 71 where the RAM Control selects a position for display (column 7, line 57- column 8, line 6));

storing at least a first portion of the active video in a video memory associated with the first VGA (Figure 12 71); and

rendering at least a second portion of the first frame of video at a second VGA in response to a second control signal (Figure 12 channel A or channel B where the picture is scrolled; Figure 16 where second portion of the first picture is rendered in second module) and storing at least second portion of the active decoded video in the memory associated with the first VGA (where the other rendered portion is stored in Display Memory section 71 and when only a two display system is used).

Noble discloses a plural display system. It is noted that Noble does not explicitly discloses a first module and a second module for displaying, however, it would have been obvious to one of ordinary skill in the art to reduce the system into only first and second modules in order to reduce the complexity of the system.

6. As per claim 2, Noble demonstrated all the elements as applied to the rejection of independent claim 21, supra, and further discloses the first portion and the second portion are the same portion (since the video data is scrolled from the first display device to the second device, the first portion and the second portion are the same portion).

7. As per claim 8, Noble demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the first VGA is a primary VGA (where Figure 11

Video Module #1 is considered primary), and the second VGA is a secondary VGA (where Figure 11 Video Module #2 is considered secondary).

8. As per claim 9, Noble demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the first VGA is a secondary VGA (where Figure 11 Video Module #1 is considered secondary), and the second VGA is a primary VGA (where Figure 11 Video Module #2 is considered primary).

9. As per claim 10, Noble demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the first VGA and the second VGA are part of a video wall such that the first frame of active video is displayed across multiple displays simultaneously (Figure 16 where a frame is displayed across multiple displays simultaneously).

10. As per claim 11, Noble demonstrated all the elements as applied to the rejected claim 21, supra, and further discloses the steps of:

receiving at the second VGA a second frame of active video from a second video source (Figure 11 since data flow is bi-directional, data flow from a Video module or Graphic Computer on the left and right is considered a first and second video source to the one in the middle); and

rendering at least a portion of the second frame of video at the first VGA (Figure 16 since the data can be scrolled, the data in the second frame of video can be in the first Video Module).

11. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al. as applied to claim 21 above, and further in view of Dennison et al. (4,729,119).

As per claim 6, Noble demonstrated all the elements as applied to the rejected claim 21, supra.

Noble discloses a system of displaying video on multiple computer displays. It is noted that Noble does not explicitly disclose the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the first VGA, however, this is known in the as taught by Dennison et al., hereinafter Dennison. Dennison discloses a memory system in which the central can be alternately used by a DMA (column 8, line 54-60).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Dennison into Noble because Noble discloses a method of displaying on a multi-display computer system and Dennison discloses the controller can be alternately used by a DMA in order to allow for faster access of the memory.

12. As per claim 7, Noble demonstrated all the elements as applied to the rejected claim 21, supra.

Noble discloses a system of displaying video on multiple computer displays. It is noted that Noble does not explicitly disclose discloses the first video memory and second video memory are accessed by a direct memory access (DMA) controller associated with the second VGA, however, this is known in the as taught by Dennison

et al., hereinafter Dennison. Dennison discloses a memory system in which the central can be alternately used by a DMA (column 8, line 54-60).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Dennison into Noble because Noble discloses a method of displaying on a multi-display computer system and Dennison discloses the controller can be alternately used by a DMA in order to allow for faster access of the memory.

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al. as applied to claim 21 above, and further in view of Lumelsky (4,949,169).

As per claim 13, Noble demonstrated all the elements as applied to the rejected claim 21, supra.

Noble discloses a system of displaying video on multiple computer displays. It is noted that Noble does not explicitly disclose the step of storing the window location in a preference file, however, this is known in the art as taught by Lumelsky et al., hereinafter Lumelsky. Lumelsky discloses in a video-graphics display window environment in which the window location is stored in a preference file ("Vertical Sample Initial Address Register (SYA) 94 and Horizontal Sample Initial Address Register (SXA) 96. These two registers specify the destination window location. Two loadable counters, Vertical Sampling Address Counter (SYCNT) 98 and horizontal Sampling Address Counter (SXCNT) 100 are used as pointers to the receiving node's frame buffer (SYADDR and SXADDR)", column 14, line 30-37).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lumelsky into Noble because Noble discloses a method of displaying video data on multiple display and Lumelsky discloses a method of tacking the window location in order to correctly display the window on different displays.

14. Claims 22 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al. (5,657,046), and further in view of Lauer et al. (5,523,769).

As per claim 22, Noble discloses a method of displaying active video on a computer system, the method comprising the steps of:

receiving at a first video graphics adapter (VGA) a first frame of active video from a video source (Figure 12 where Channel A and B are inherently connected to a video source); and

displaying at least a first portion of the first frame of video at a second VGA in response to a second control signal (Figure 16 where second portion of the first picture is rendered in second module), wherein the second control signal is a signal specifying a window location for displaying the active video (Figure 12 RAM Control to the Display Memory Section 71 where the RAM Control selects a position for display (column 7, line 57- column 8, line 6)).

Noble discloses a plural display system. It is noted that Noble does not explicitly discloses a first module and a second module for displaying, however, it would have been obvious to one of ordinary skill in the art to reduce the system into only first and second modules in order to reduce the complexity of the system.

Noble discloses a system of displaying video on a computer display. It is noted that Noble does not explicitly disclose the video source is at least one of the following: a video decoder and a television signal. However, this is known in the art as taught by Lauer et al., hereinafter Lauer. Lauer discloses a multiple display system in which "each individual unit or a subgroup is arranged to have its associated module with its own integral processor and memory responsible for font and graphics rendering, image processing, video decoding, clipping and coordination with adjacent modules", column 5, line 5-10.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Lauer into Noble because teaches a system of displaying video on multiple computer system and Lauer teaches the video source can be a coded signal can be decoded by the decoding module in order to be able to decoding coded signals.

15. As per claim 17, Noble and Lauer demonstrated all the elements as applied to the rejection of independent claim 22, supra.

As for the video decoder is for decoding a compressed video signal, it is inherent that a video signal to be decoded is a compressed signal.

16. As per claim 18, Noble and Lauer demonstrated all the elements as applied to the rejection of independent claim 22, supra, and Noble further discloses the video source sending the first frame of data over a bus local to the first VGA (Figure 12 bus line between 71 and 7).

Response to Arguments

17. Applicant's arguments filed 5/10/2004 have been fully considered but they are not persuasive.

As per claims 13 and 21, Applicant alleges Noble does not disclose 1) a first control signal being a signal specifying a window location for display active video and 2) storing at least second portion of the active decoded video in the video memory associated with the first VGA. In reply, examiner the RAM Selects line in Figure 12 specifies a window location for display active video, and when the number of display is reduced into two, and since the system has scrolling operation, hat is displayed in the first display could be stored in the second memory.

Applicant's arguments with respect to claims 6-7 have been considered but are moot in view of the new ground(s) of rejection.

As per claims 8 and 9, since applicant does not distinguish a primary VGA or secondary VGA, examiner considers they can be arbitrary named.

As per claim 11, examiner considers the system can be reduced to a system of two displays and the corresponding display modules and the limitations are met when the video data is scrolled (part of the video image in the first module is in the second module and vice versa).

As per claim 22, examiner considers the RAM selects (Figure 12) calculates the position of the pixel to be displayed.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiries

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ryan Yang** whose telephone number is **(703) 308-6133**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Michael Razavi**, can be reached at **(703) 305-4713**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-47000377.

Ryan Yang
July 29, 2004

JEFFERY BRIER
PRIMARY EXAMINER